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Notice of Allowability	Application N .	Applicant(s)	
	10/671,654	CHEN ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the corresp ndence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amdt (Aug 24, 2005)*.

2. ☒ The allowed claim(s) is/are *1-4, 6, 8-12, and 14-19 (now renumbered as 1-16, respectively for printing purposes)*.

3. ☒ The drawings filed on *04 April 2005* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Claim 3, line 7: changed "a voltage" to --the voltage--;

Claim 11, line 3: changed "a first voltage" to --the first voltage--;

line 7: changed "a second voltage" to --the second voltage--; and

Claim 18, line 3: changed "a voltage" to --the voltage--.

Each of the changes to the claims above addresses/corrects a minor oversight, wherein after an independent claim had a "voltage supply" phrase added to it, the associated "voltage supply" phrase within its dependent claim (i.e. "a voltage supply" as recited within each of claims 3 and 18; or "a first voltage supply" and "a second voltage supply" as recited within claim 11) should also have had a corresponding change made. [For example, claim 1 now recites "a voltage supply" and "the voltage supply" on lines 16 and 39, respectively. Therefore, "a voltage supply" in dependent claim 3 was amended to clearly refer back to the "voltage supply" now cited in claim 1, thus minimizing possible confusion with respect to how many voltage supplies were being recited.]

RESPONSE TO AMENDMENT

The amendment submitted on Aug 24, 2005 has been reviewed and considered with the following results:

The cancellation of claims 5, 7, 13, and 20 rendered their respective objection and/or rejection moot.

Amended claims 4 and 11 overcame the objections to claims 4, 6, and 15, which have now all been withdrawn.

Amended independent claims 1, 8, and 16 overcame the rejections of claims 1-4, 6, 8-12, 14, and 16-19 under 35 U.S.C. 102(b). Therefore, those rejections have been withdrawn. Takeyabu does not show/disclose the gate of at least one input mirror transistor being coupled to the drain of its corresponding input cascode transistor as now recited within each of the independent claims.

Although several minor oversights were noted, with respect to some amended claims, these were all addressed/corrected by the Examiner's Amendment described above.

Therefore, there is no known objection or rejection remaining within the present application.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

None of the prior art references reviewed and considered shows or discloses a charge pump as recited within independent claims 1, 8, and 16. Although some references show the first/second cascode current mirrors (with all of their corresponding input/output transistors (i.e. mirror and cascode transistors)), and the first/second switching transistors, none of the prior art references clearly shows/discloses the drain of an input cascode transistor being coupled to the gate of its corresponding input mirror transistor as recited within claims 1 (upon which claims 2-4, and 6 depend), 8 (upon which claims 9-12, and 14-15 depend), and 16 (upon which claims 17-

19 depend), wherein a switching transistor is coupled between its corresponding output mirror/ cascode transistors. Since there is no strong motivation (as described later) to modify or combine any prior art reference(s) to ensure the charge pump meets all of the claimed limitations, including the specific drain to gate coupling as described above, the claims are deemed patentably distinct over the prior art of record.

Claims 1-4, 6, 8-12, and 14-19 are allowed, and have been renumbered as 1-16, respectively for printing purposes. The renumbering takes into account the cancellation of claims 5, 7, 13, and 20.

PRIOR ART

The two prior art references on the accompanying PTO-892 are cited for interest and documentation purposes only. Both were found during the recent update search, and each shows an example of cascoded current mirrors wherein the gate of one input mirror transistor is coupled to the drain of a corresponding input cascode transistor. Ide's Fig. 3 shows a conventional cascoded current mirror comprising current source 111 coupled in series with diode-connected input cascode transistor Mi112 and diode-connected input mirror transistor Mi111, which form current mirrors with transistors Mo112 and Mo111, respectively. Fig. 6 shows a variation of the five-element structure (i.e. one current source and four transistors), wherein the gate of input mirror transistor Mi11 is now coupled to the drain (and gate) of input cascode transistor Mi12. Ide discloses that Mi12 has a low threshold voltage, and Mi11 has a high threshold voltage (e.g. see column 12, lines 12-16). Fig. 2 of Pauls also shows a conventional five-element cascoded current mirror corresponding to Ide's Fig. 3. Pauls' variation, shown in Fig. 5, shows the gate of input mirror transistor MN7 coupled to the drain of input cascode transistor MN8, plus two

additional elements (i.e. current source Ibias and diode-connected transistor MN11). This Fig. 5 cascode current mirror is disclosed as having "a high output resistance and a low swing output voltage" (e.g. see column 3, lines 66-67). However, there is no strong motivation to use either of these references to modify Takeyabu's circuit (used in the previous Office Action's rejections of various claims) to ensure the gate of the input mirror transistor is coupled to the drain of the input cascode transistor as recited within the claims. For example, Ide's variation would couple the gates of all four transistors together with the drain of transistor Mi12. However, since Takeyabu's cascode current mirror also comprises switching transistor NT14 between transistors NT15 and NT13 (e.g. see Fig. 16), it is not clear if such a Takeyabu/Ide type circuit would function properly. As for Pauls' variation, it would add an additional current path with additional components (i.e. Ibias and MN11). Therefore, this configuration would consume more energy (i.e. within the additional current path), and take up more area (i.e. additional components), which effectively teaches away from the typical desire of conserving energy, and using as little space as possible within integrated circuits.

The reference of Warner, cited by the examiner in a previous Office Action, also shows the gate of input mirror transistor 78 being coupled to the drain of input cascade transistor 76 in Fig. 2. However, this reference lacks any clear description of any advantage such a connection has, and switching transistor 54 of the cascode current mirror (e.g. 76,78,62, and 64) is not shown between transistors 62 and 64. Therefore, there is no strong motivation to modify this reference to ensure all the limitations recited within any of the present application's independent claims are met. Also, there is no strong motivation for applying the gate to drain type connection of Warner to Takeyabu's circuit.

Any comments considered necessary by the applicants must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Terry L. Englund

9 September 2005